Applied Engineering and Technology Directorate

Interface Control Document Between the Ultra Long Duration Balloon (ULDB) Balloon-Craft Flight Computers and the ULDB Support Subsystems

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Interface Control Document Between the Balloon-Craft Flight Computer and the ULDB Support Subsystems

Revision 1

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1.0 Introduction

1.1 Purpose

The Purpose of this document is to provide a detailed description of the electronic interface between the Ultra Long Duration Balloon (ULDB) flight computer and the ULDB Standard Instrumentation Package (SIP) subsystems.

1.2 Scope

This Interface Control Document (ICD) defines and controls the communications, format, protocol, messages, electrical and mechanical characteristics of the interface between the ULDB flight computer and the SIP subsystems.

1.3 Time Frame

This ICD shall be in effect from the date of approval by the Balloon Program Office, the Real Time Software Engineering Branch; and when all applicable signatures are obtained.

2.0 Applicable Documents

2.1 General

This section lists the standards, specifications, and other documents which serve as a reference for supplemental system and subsystem descriptive information. Other documents listed are directly applicable to this ICD and may by specific references constitute a part of this ICD.

2.2 Specifications

a. ULDB Flight Software Requirements and Functional Specifications, Ver. 1.1
b. ULDB Design to Requirements Document (DTRD), 820-ULDB-DTRD-002.1
c. ULDB Control Center Requirements and Functional Specifications, Ver.

2.3 Standards

a. MIL-STD-1553B
b. Consultative Committee for Space Data Systems (CCSDS) - Packet Telemetry, CCSDS 102.0-B-4, Blue Book, November 1995
c. Electrical Characteristics of Balanced Voltage Digital Interface Circuits, EIA RS-422A (Federal Standard 1020A), Electronic Industries Association, Washington, D.C.

2.4 Other Documents

a. Motorola Fourth Generation TDRSS User Transponder User's Guide, DWG #12-P40009E, Rev. XB
b. User Manual for the Telonics ST-13 Asynchronous Serial Interface, PB005443, 08/04/1997

3.0 ARGOS

3.1 General Description

The ARGOS communication link serves as a global data downlink transmission only. The flight computer interfaces to a platform-transmitting terminal (PTT) via an RS232 connection. Telonics makes the PTT and has called it the ST-13. The ARGOS Service Network operates the ARGOS satellite network in a random access mode.

3.2 ST-13 Software Configuration

This section detail's the factory set features available on the Telonics ST-13 transmitter. More information can be obtained by accessing the User Manual for the Telonics ST-13 Asynchronous Serial Interface.

3.2.1 ID Codes

The ARGOS satellite network sorts data received by assigning unique ID codes. The ULDB mission makes use of each ID code to maximize housekeeping data and structure data in accordance with each ID. Eight ID codes have been programmed into the PTT at the factory with a data transmission capability of 32bytes/ID, and has assigned the ULDB mission 16 unique IDs. Each ST-13 has factory set 8 of these assigned ID codes. A total of two ST-13s, one for each flight computer, shall be active at all times. The ID code assignments are listed below

ID#	Hex	Decimal	Transmitter #
1	92010	9344	1
2	93F09	9468	1
3	9457C	9493	1
4	959E2	9575	1
5	9741E	9680	1
6	97A51	9705	1
7	97B4E	9709	1
8	98BD8	9775	1
9	92043	9345	2
10	93F5A	9469	2
11	94589	9494	2
12	95A36	9576	2
13	9744D	9681	2
14	97AA4	9706	2
15	97BBB	9710	2
16	98C23	9776	2

The flight computer will place a CCSDS header in each ID. The header will identify the type of data contained within the ID.

3.2.2 Repetition Rate

Each transmission of data shall be repeated with new data every 60 seconds. The flight computer should space out ID transmissions every 7 seconds and not repeat any single ID transmission any sooner than 60 seconds. The transmitter requires a minimum of 1 second for a complete data transmission of one ID.

3.2.3 FailSafe Mode

The FailSafe mode allows users to know when the host has stopped communications with the transmitter. The FailSafe mode will become active once it is enabled, the host has not successfully commanded the ST-13 longer than the factory set time out interval, and the unit is not operating in the "automatic repeat transmission" mode. The FailSafe mode is factory set to be enabled upon powering the unit up and can be toggled on or off by the host

3.2.3.1 FailSafe IDs

Each transmitter for the ULDB mission contains separate FailSafe mode IDs that identify a "FailSafe" mode condition. Below is a table listing of these IDs.

Transmitter #	Decimal	Hex
1	9305	9167C
2	9306	91689

3.2.3.2 FailSafe Repetition Rate

The FailSafe repetition rate is the interval at which a FailSafe ID and message will be repeated. The factory setting for both ST-13 units is 60 seconds.

3.2.3.3 FailSafe Timeout Interval

The FailSafe timeout interval is the amount of time elapsed with no host communications with the ST-13. The factory setting for both units is 60 minutes.

3.2.3.4 FailSafe Message Length

The FailSafe message length allows users to annotate a unique message of up to 28 bytes for all FailSafe mode transmissions. The first four bytes of all FailSafe messages always contain an error count and up to four of the most recent error codes. The factory setting chosen for the FailSafe message length on both units is 0 bytes. The ID will be used to identify this mode with no other message format required.

3.2.3.5 FailSafe Duty Cycle

The FailSafe duty cycle allows for periods of FailSafe mode on and off time. The factory setting chosen for the FailSafe mode duty cycle is continuous. The host is required to re-establish communications with the ST-13 to disable FailSafe mode transmissions. The ST-13 can be powered off if communications cannot be re-established.

3.2.4 Transmit Error Counts Mode

The "Transmit Error Counts" allow the user to track any transmission errors. The first 4 bytes of each transmitted message contain the error count plus the most recent error codes. The user can enable this mode as on or off.

3.3 Message Formats

Three distinct message formats are identified for transmission: "FailSafe" mode, "Transmit Error Counts" mode, and a message format without "Transmit Error Counts" mode. Figures 1-3 identify each of these message formats.

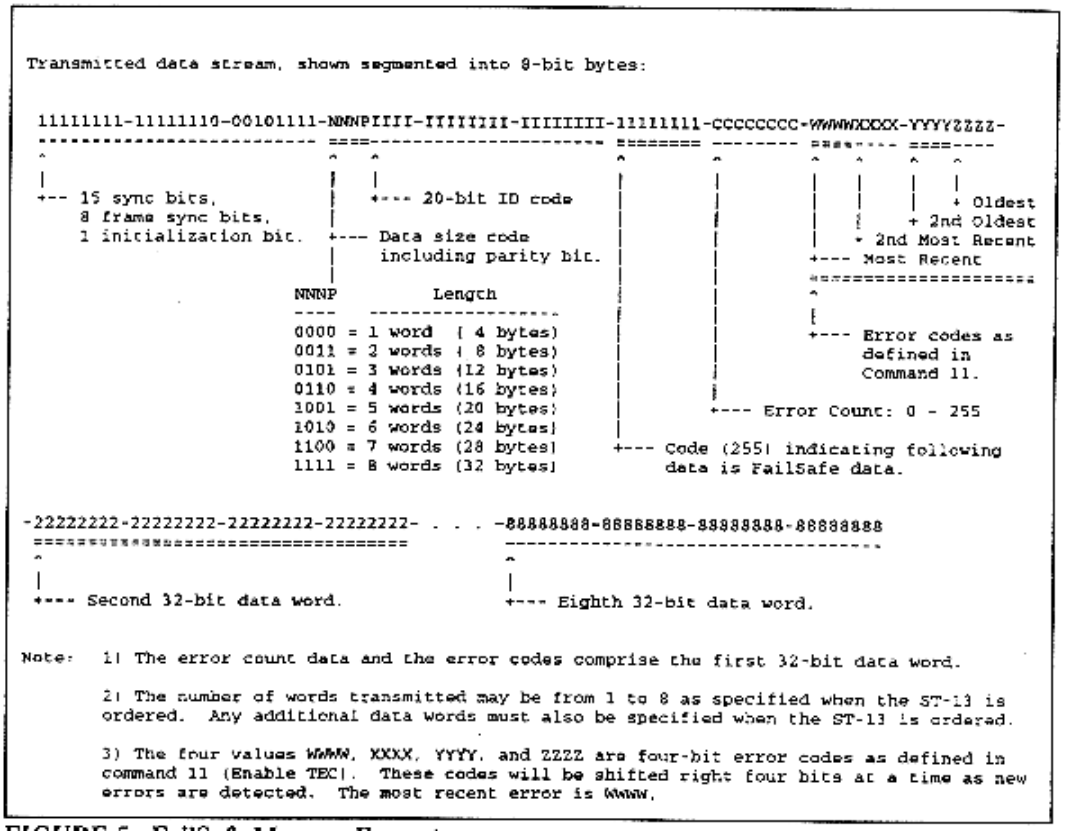


Figure 1: FailSafe Mode Transmission Format

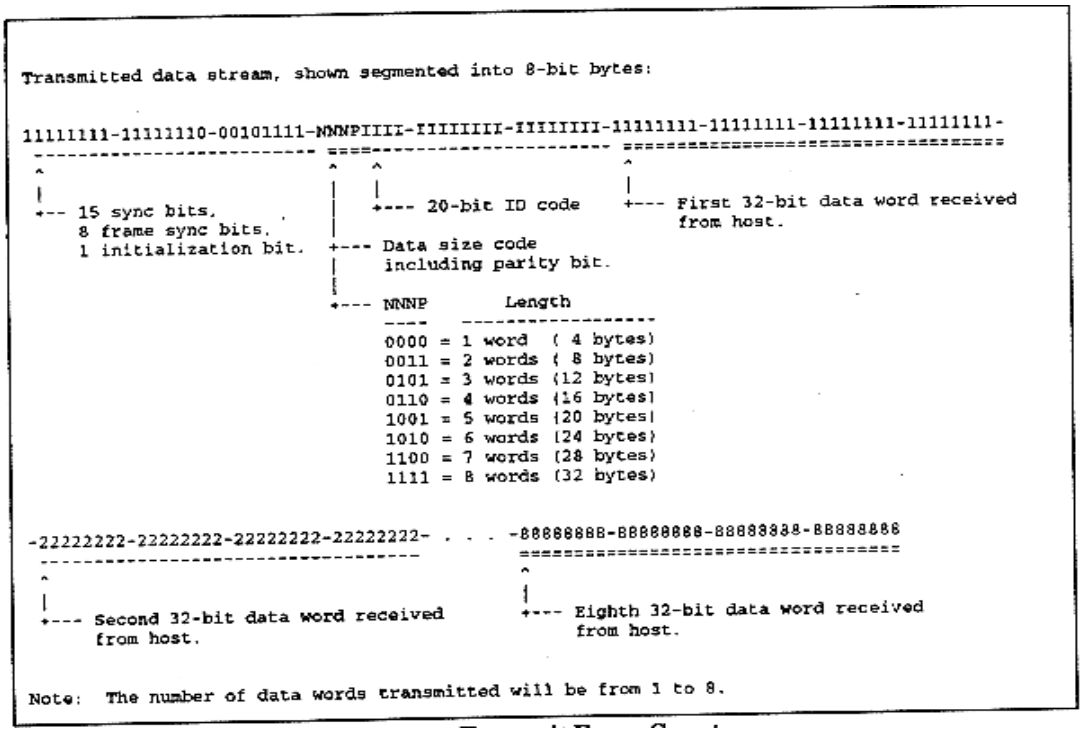


Figure 2: Message Format with Transmit Error Counts

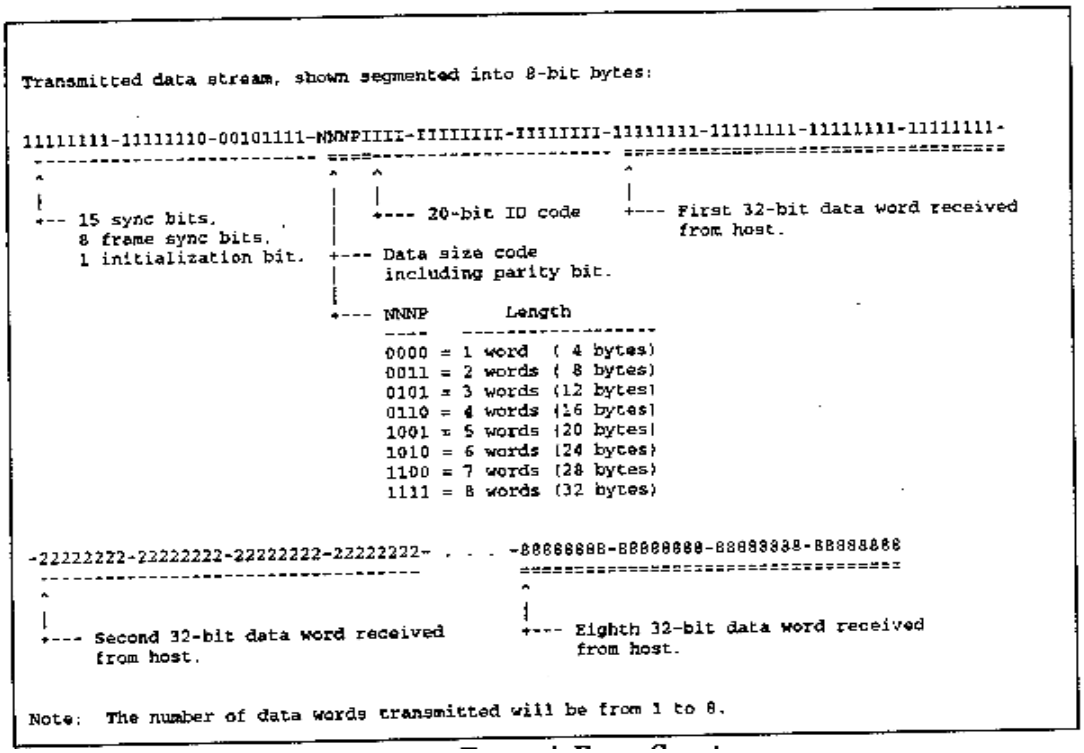


Figure 3:Message Format without Transmit Error Count

3.4 ST-13 Hardware Configuration

The hardware connection for the ARGOS communication link is via an RS-232 link from the flight computer to the Telonics ST-13. Below is a pinout of the Telonics ST-13 DB-25 female connector.

Pin 1: Async Wake-up Signal
RS-232: This line is pulled to ground through a 30K Ohm resistor. The idle state of this line is low (0 to –15V). Pulling this line high (+5 to +15V) will cause a wake-up interrupt in the ST-13.

Pin 2: TXD: Used to transmit Data to the ST-13
RS-232: This line is driven by an RS-232 line driver. When the ST-13 is awake and communicating with the host, the idle state of this line is low (-5 to –15V). Start bits and Zero bits are transmitted with this line in the high state (+5V to +15V). One bits are transmitted with this line in the low state(-5 to –15V). Note that when the ST-13 is not communicating with the host (i.e. between commands), the RS-232 driver chip is powered down to save battery power. This causes the TXD pin to be pulled toward 0V. The host system must be aware of this and disable its receiver during this time.

Pin 13: Common ground for transmit, receive and wake-up signals.

Pin 14: RXD: Used by the ST-13 to receive data from the host.
This line is connected to a RS-232 line receiver which has an internal 5K Ohm resistor to ground. The host should hold this line low (-5 to –15V) for the idle state and for one bits. This line should be driven high (+5 to +15V) for start bits and zero bits.

Pin 22: CR: +5 V source used in some application requiring pull-ups.

Pin 11, 23: - Battery: Negative Power Applied

Pin 12, 24: + Battery: Positive Power Applied

Pin 25: Digital Ground

3.5 ST-13 Electrical Interface

Figure 4 illustrates the termination of the serial I/O pins internal to the ST-13 for the RS-232 interface. Each pin is RF filtered and the wake-up pin has 30K Ohms of resistance to ground. The TXD and RXD pins come directly from an RS-232 driver/receiver chip. Note that this chip is powered on when a wake-up signal is received, and powered off after reception of the complete command from the host. The flight computers TX and RX lines should be connected to the RXD and TXD lines of the Argos Transmitter respectively. Grounds should be shared accordingly. Pinout descriptions are described under section 3.4 Hardware Configuration.

3.6 Protocol

The serial communication protocol for the Telonics ST-13 is the following:

a. Asynchronous serial utilizing standard NRZ format.
b. One start bit, eight data bits, one stop bit, no parity.
c. Baud Rate = 2400
d. Data is transmitted least significant bit first.

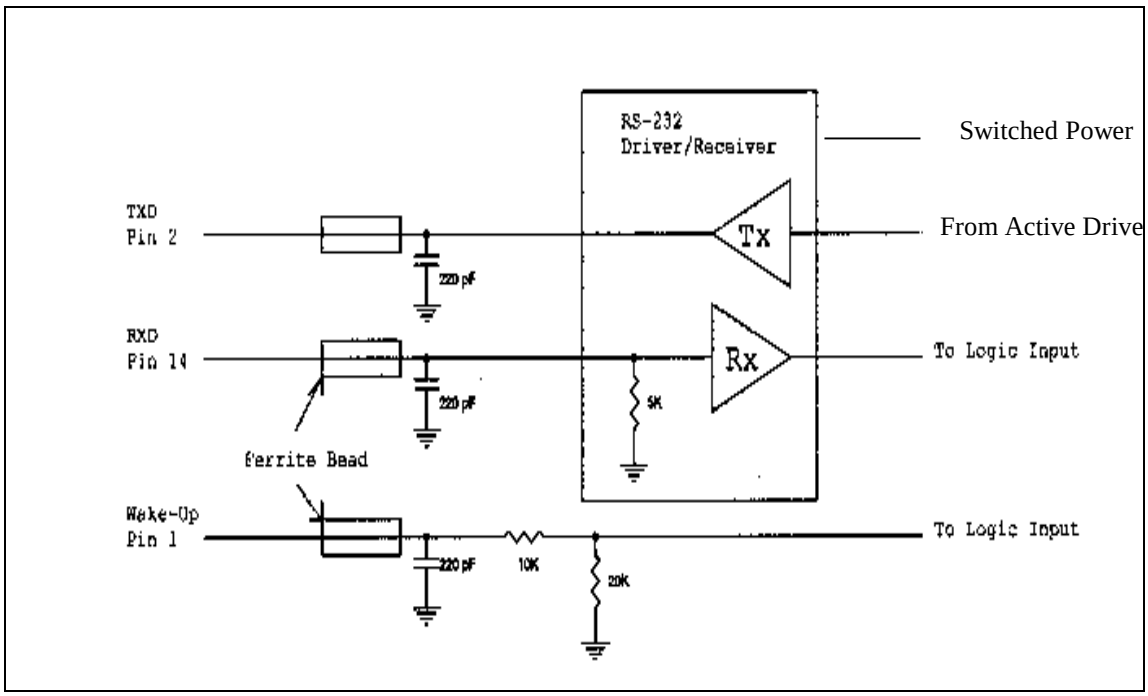


Figure 4: Serial I/O, RS-232 Termination

3.7 Commanding

Commanding the ST-13 is performed by the bi-directional RS232 connection. All commands received by the ST-13 are acknowledged by an ACK while those commands not recognized are acknowledged by a NAK. Use of the acknowledgement commands is accomplished by connecting the ST-13's TXD line to the host UART's RXD pin.

Commands sent by the flight computer to the ARGOS transmitter (ST-13) consist of a command byte specifying the function to be performed and an ID code that associates the data being transmitted. Specifying an ID code is accomplished by passing a number between 0 and 7 that acts as an internal lookup table of stored ID codes in the ST-13.

3.7.1 Command Data Format

The host must send the ST-13 command bytes and data bytes in the format of 8-bit binary. The host UART must configure to send 8-bit binary with no parity.

3.7.2 Command Initiation

All commands are initiated by the host sending a momentary active high signal for an RS232 connection that last for 25-100 milli-seconds on the wake-up line of the ST-13. The wake-up signal line must return to the idle state before serial data and command byte transmissions can occur. The ST-13 will respond with an ACK (00000110) for valid commands and a NAK (00010101) for non-valid commands. The ST-13 enters a sleep mode and must be re-awakened before any other commands can be transmitted from the host.

A delay of 100 milli-seconds is required between the last byte received by the ST-13 and the next wake-up pulse for the following command. A delay of up to 3 seconds may be required for initiating transmission commands.

3.7.3 ST-13's Acknowledgement

The ST-13 should respond with every host command sent to it with either ACK (00000110) or NAK (00010101). However, the ST-13 should be re-awakened and the command retransmitted if after 3 seconds the host has not received an acknowledgement. If 5 attempts to transmit the same host command have failed, a serious interface problem exits (such as moisture penetration). The host should abort any further attempts and try later to send the command in hopes that the problem has corrected itself.

3.7.4 ST-13 Time Out

The ST-13 uses a "watch dog" timer once it receives a wake-up signal. If within 2 seconds the ST-13 does NOT receive a command byte and any required data bytes a series of events begin:

a. A time out situation is declared.
b. The read operation by the ST-13 is aborted.
c. The ST-13's internal error counters are incremented.
d. A NAK is sent to the host.
e. The ST-13's RS232 driver/receiver chip is powered down.
f. The ST-13 goes back to sleep.

3.7.5 Commands

Eight bit binary commands define how the ST-13 is to perform. Below is a table listing of the commands available and a description.

3.7.5.1 Transmit and Store Commands

The Transmit and Store commands describe how the ST-13 stores data in its buffers, transmits data, and combines both store and transmit capabilities.

3.7.5.1.1 Store Data 1

Format: 00010xxx

The Store Data 1 commands the ST-13 to store 8-bit binary data to buffer number 1 in the ST-13, but do not transmit. The "xxx" value varies from 0 (000) to 7 (111) and refers to the index of 8 possible ARGOS ID codes programmed by the factory in an internal look

up table of the ST-13. This allows the host's data to be identified with a particular ARGOS ID when the data is transmitted.

The amount of data bytes/ID is 32. The ST-13 error counter is incremented when the host does not send enough data bytes. The operation will then be aborted and buffer number 1 is marked as containing no data. The Auto-Repeat function will be canceled if active to eliminate any invalid data. If the host sends more data than that required by the ARGOS ID code factory setting, the excess bytes are ignored and the initial amount is placed in buffer #1 while no error code is generated. The table below details how the ST-13 index corresponds to the command.

Binary CMD	Hex CMD	Decimal CMD	ID Index
00010000	$10	16	1
00010001	$11	17	2
00010010	$12	18	3
00010011	$13	19	4
00010100	$14	20	5
00010101	$15	21	6
00010110	$16	22	7
00010111	$17	23	8

3.7.5.1.2 Store Data 2

Format: 00100xxx

The Store Data 2 command places data bytes into buffer #2 of the ST-13, but does not transmit. The same conditions exist for this command as did the Store Data 1 command.

3.7.5.1.3 Store and Transmit 1

Format: 00110xxx

The Store and Transmit 1 command store data in buffer #1 and immediately transmits the data. The time between command initiation and transmission completion can be up to 8 seconds. No commands must be initiated for buffer #1 while this command is active to ensure transmission of buffer #1 is complete.

3.7.5.1.4 Store and Transmit 2

Format: 01000xxx

The Store and Transmit 2 command is performed in the same manner as the Store and Transmit 2 command except data is stored in buffer #2 before transmission.

3.7.5.1.5 Transmit 1

Format: 01010xxx

The Transmit 1 command transmits previously stored data from buffer #1. No data follows this command. The "xxx" value corresponds to the index of 8 different (0-7) ARGOS ID codes. The command operation will be aborted and the error counter incremented if the amount of data stored in buffer #1 is different than the factory programmed message length for that ARGOS ID. The ULDB mission uses 32 bytes/ID for all ARGOS ID codes. A total of 8 seconds is required to complete the command

initiation to completion of transmission. No other commands should be initiated during this time that involve buffer #1 to ensure all of buffer #1 contents is transmitted.

3.7.5.1.6 Transmit 2

Format: 01100xxx
The Transmit 2 command transmits previously stored data from buffer #2. The same conditions exist for this command as the Transmit 1 command except the Transmit 2 command uses buffer #2 to transmit data.

3.7.5.2 Auto-Repeat

Format: 0110zyx
The Auto-Repeat command allows RF transmissions to be repeated at default or programmable intervals automatically. This command uses 1 to 3 bytes depending upon if the ST-13 default values are used for repetition rate and repetition count. The Auto-Repeat command will consist of 1 byte if bit y = 1. Otherwise, the Auto-Repeat command will consist of 3 bytes whereby bit y = 0 and the host supplies the command, repetition rate, and the repetition count.

The least significant bit (LSB) of the first command byte, x, specifies which buffer to extract data from. Buffer #1 will be repeated if x = 0 while buffer #2 will be repeated if x = 1. Buffer #1 and buffer #2 will be alternately repeated if bit z = 1. The command byte LSB dictates which buffer to begin alternating if bit z = 1.

The second command byte (if used) identifies the repetition rate in seconds added to a 42-second base. The minimum repetition rate of 0 seconds indicates a total repetition rate of 42 seconds while the maximum repetition rate of 255 indicates data to be repeated at 297 (255+42) second intervals. The final command (if used) identifies the number of repetitions (1 to 255). This final command requires the buffer to be preloaded using the Store Data 1 or Store Data 2 command. A NAK will be sent to the host and the system error counter incremented if the specified buffer is not previously setup.

The repetition rate and repetition count normally supplied in bytes 2 and 3 are stored as default values in the ROM of the ST-13. The default total repetition rate and repetition count for both ST-13s on the ULDB mission are 60 seconds (42+18) and 1 count. The factory sets the default settings at the time of order.

3.7.5.3 Cancel Auto-Repeat

Format: 10000000
The Cancel Auto-Repeat command terminates an Auto-Repeat command before it completes all of its programmed iterations. The Cancel Auto-Repeat command is required to cancel any Auto-Repeat operations before loading new data into the buffers.

3.7.5.4 Null Command

Format: 10110000
The Null command does not cause a transmission and should be used by the host to let the ST-13 know the host is alive. Otherwise, the ST-13 will enter a FailSafe mode. The

ST-13 responds by sending an ACK to the host letting the host know everything is OK with serial interface.

3.7.5.5 Disable TEC
Format: 11000000
The Disable TEC command disables the "Transmit Error Counts" mode. Details of the TEC mode are discussed under the Enable TEC command.

3.7.5.6 Enable TEC
Format: 11010000
The Enable TEC command enables the "Transmit Error Counts" mode. The "Error Count Marker"(1byte), the "Error Count"(1byte), and the four most recent error codes (2-bytes) are enabled into the ARGOS data stream. The TEC mode message format is presented in Figure 2. Below is a listing of the 4-bit error codes and their definitions.

Binary Error Code	Description
0000	No error (OK)
0001	FailSafe Timeout
0010	Illegal command from host
0011	ARGOS ID Code index not legal. The index value is greater than the number of ID Codes stored in the ST-13.
0100	Size of data residing in requested buffer is inconsistent with the specified ARGOS ID.
0101	Host took more than 2 seconds to complete transmitting data following "wake-up" signal to ST-13.
0110	ST-13 UART detected overrun
0111	ST-13 UART detected line noise
1000	ST-13 UART detected a framing error (stop bit not in position)
1001	Auto Repeat – Buffer requested by host not valid (does no contain any data)
1010	Auto Repeat -- Zero transmission iterations specified by host

3.7.5.7 Disable FailSafe
Format: 11100000
The Disable FailSafe command disables the FailSafe mode. This command requires the 16 bytes of hexadecimal qualification data following the binary command. The qualification data is the following: AA, AA, AA, AA, AA, AA, AA, AA, AA, AA, AA, AA, AA, AA, AA, AA. This command resets the internal counter, which controls the FailSafe duty cycle.

3.7.5.8 Enable FailSafe
Format: 11110000
The Enable FailSafe command enables the FailSafe mode. The internal time counters controlling the FailSafe duty cycle are started but not reset. Figure 1 displays the message format when the ST-13 is in the FailSafe mode. The first word following the FailSafe ID code is always the "Error Counts" followed by the 4 most recent error codes.

4.0 TDRSS Command

4.1 General Description

The TDRSS Command interface to the flight computers receives commands asynchronously from the system stack's command decode deck. A lock detection bit from the TDRSS transceiver indicates incoming command data is ready to be clocked into the command decode deck of the system stack. The command decode deck re-formats command data into an asynchronous RS232 stream at 300 baud into the flight computer(s) comm port.

4.2 TDRSS Command Data Flow

The flight computer receives all TDRSS commands via a dedicated RS232 comm port. The TDRSS transceiver uses a detection bit to tell the command decode deck that a command has been received. The command decode deck synchronously extracts the command from the TDRSS transceiver via RS422 and reformats it into the standard 8-byte command format using asynchronous RS232 at 300 baud to the flight computer(s). A switch enables the TDRSS command(s) to flow from the command decode deck into either flight computer #1 or #2.

4.3 Electrical Interface

The flight computer uses an asynchronous RS232 connection to the TDRSS Command Decode deck. Commands are sent from the system stack command decode deck to the flight computer. The RS232 driver/receiver chip (Maxim 233) on the command decode deck transmits with a maximum voltage output swing of ±15V and is loaded with a 3kΩ to ground resistor.

4.4 Hardware Configuration

The system stack command decode deck interface is a DB9P connector with a dedicated RS232 output to the flight computer(s). Below are the pin-outs for the command decode deck and the flight computer(s).

FLIGHT COMPUTER	PIN #
Computer #1 RXD	TBD
Computer #2 RXD	TBD
Computer #1 Ground	TBD
Computer #2 Ground	TBD

COMMAND DECODE DECK	PIN #
Transmit Out	2
Ground	5

4.5 Protocol

The TDRSS Command Interface protocol for the flight computer is the following

a. Asynchronous serial utilizing standard NRZ format.

b. One start bit, eight data bits, one stop bit, and no parity.
c. Baud Rate = 300
d. Data is transmitted least significant bit (LSB) first.

4.6 TDRSS Command Format

Commands received from the TDRSS Command Decode deck are in a standard 8-byte command format. See Appendix A for details. The TDRSS Command format provides 2 command bytes per packet. Command byte 1 is the command ID, allowing 256 discrete commands to be identified. Command byte 2 is the data argument for command byte 1. The entire 8-byte packet is forwarded to the appropriate subsystem once the flight computer receives a command packet whose routing ID matches that subsystem. See appendix A for a complete list of all routing IDs.

5.0 TDRSS ACU

5.1 General Description

The flight computer interface to the TDRSS Antenna Control Unit (ACU) relays status information on the TDRS ACU and routes commands to the TDRSS ACU.

5.2 Electrical Interface

6.0 TDRSS Data Interface

6.1 General Description

The TDRSS data interface (TDI) is a PC-104 card that resides in the flight computer. The TDI acts as a continuous data buffer for science and housekeeping from the flight computer to the TDRSS transponder. All science data shall flow through the TDI before being transmitted through the TDRSS transponder. The TDI uses the PC-104 architecture bus for addressing and data flows.

6.2 Electrical Interface

The electrical interface to the TDI board uses the +5V TTL lines from the PC-104 bus to drive the CMOS and TTL logic. The PC-104 AT Bus expansion connector shall be connected to the TDI board. The TDI has four compatible RS-422 differential line drivers that output data to the TDRSS transponder. The differential RS-422 telemetry data entering the TDRSS transponder from the TDI uses MC26C31 line drivers with 100Ω series resistors, and is compatible to the EIA RS-422A electrical standard. The TDRSS transponder requires no RS-422 protocol and uses only the differential electrical interface. 200Ω series terminating resistors are used in the TDRSS transponder. Pinouts for the TDI board share the same pin-outs from the flight computer AT bus expansion connector given in section 6.9 Hardware Configuration.

6.3 Data Flow

A continuous science and housekeeping data stream from 0 to 150Kbps shall be achieved by flowing data acquired from the flight computer through the TDI board. Data flows shall use the 8-bit PC-104 parallel data bus. The flight computer writes data to FIFO (First in First Out) buffer chip(s), IDT7208, on the TDI. Data entering the TDRSS transponder is combined QPSK and requires an I and Q channel data stream. Parallel data enters the FIFO(s) while CMOS and TTL logic serial streams data to 422 line drivers that drive data to the TDRSS transponder. The same data shall exist on each I and Q data channel stream into the TDRSS transponder.

6.4 Operating Mode

The TDI board operates in the combined QPSK mode only. Both the I and Q channels contain the same data. Data entering the TDI via the 8-bit data bus is placed on the main FIFO buffer and a backup FIFO simultaneously. The Main FIFO dumps data into both the I and Q channels of the A bus of the TDRSS transponder while the backup FIFO places the same data on the secondary B bus of the TDRSS transponder. It is left to the flight software to identify data as Real-time (R/T) or playback (P/B).

6.5 I/O Base Address

The TDI board uses the PC-104 bus expansion address pin-outs SA3-SA10 as an address base, which is DIP switch selectable on the board. An 8-bit comparator is used to ensure proper I/O base addressing. The TDI I/O base address setting is TBD.

6.6 Write and Reset

The flight computer is required to use 2 address lines for writing and resetting data to the main and backup FIFO(s). The address lines used are the 2 Least Significant Bits (LSBs) of the PC-104 flight computer's address, SA0 and SA1.

6.6.1 Data Writes

Data written to the TDRSS Data Interface board is addressed from the PC-104 flight computer address bus. The flight computer must place 8-bit data on the PC-104 data bus before the command is given to write the data to the appropriate FIFO. Data writes are made simultaneously to both the main and backup FIFO by placing a binary 00 in the 2 LSBs of the PC-104 flight computer's address.

Function	SA1	SA0
FIFO write	0	0

6.6.2 FIFO Reset

Parallel data entering the FIFO(s) can be reset or cleared by initiating a reset. This is accomplished by a software address write or a hard-drive reset. A software FIFO reset is accomplished by placing a binary 01 in the 2 LSBs of the PC-104 flight computer's address.

Function	SA1	SA0
FIFO reset	0	1

A reset is required on both FIFOs upon power up before a write operation can take place.

6.7 Data Rate Selection

The TDI board uses a programmable external crystal oscillator (PXOs) to clock data out to the TDRSS transponder. The flight computer shall set the PXO clock frequency to two times the commanded data rate desired. If the desired data rate output is 50KHz, the flight computer shall program the PXO for 100KHz. This is done to achieve the 2X clock required for convolutional encoding on the TDI board.

6.7.1 Data Clock Enabling

The first six bits of the PC-104 data bus are used to program the PXO clock frequency. The flight computer must place a binary 10 into the 2 LSBs of the flight computer's address to enable data onto the PXO control lines.

Function	SA1	SA0
Enable PXO Control Lines	1	0

Data should first be placed on the first 6 bits (SD0-SD5) of the PC-104 data bus before enabling the PXO control lines to the PC-104 data bus. The next section 6.7.1 entitled,

PXO Control Settings, details how and what to place on the PC-104 data bus to program the desired frequency.

6.7.2 Clock Frequency Setting

There are 57 discrete frequencies available on each PXO. Below is a table summarizing the different frequencies available. The PXO chosen for this mission uses an external 20MHz crystal oscillator at ±25ppm.

Set of Output Frequencies

CTL1	CTL2	CTL3	Dividing Ratio	CTL4	CTL5	CTL6	Dividing Ratio
0	0	0	1/1	0	0	0	1/1
0	0	1	1/10	0	0	1	1/10
0	1	0	½	0	1	0	$1/10^2$
0	1	1	1/3	0	1	1	$1/10^3$
1	0	0	¼	1	0	0	$1/10^4$
1	0	1	1/5	1	0	1	$1/10^5$
1	1	0	1/6	1	1	0	$1/10^6$
1	1	1	1/12	1	1	1	$1/10^7$

Example:
If the desired frequency is 50KHz then the programmed frequency must be 100KHz. Using the 20MHz base frequency requires placing a binary 010010 on SD5 – SD0. The first 3 control lines of the PXO divide the external crystal oscillator by ½ yielding 10MHz. The last 3 control lines divide 10MHz by 100 to give 100KHz.

Frequency	SD5	SD4	SD3	SD2	SD1	SD0
100KHz	0	1	0	0	1	0

6.8 Status Flags

The FIFO(s) have three status flags indicators; Full Flag (FF), Empty Flag (EF), Half Full Flag. The flight computer must place a binary 11 into the 2 LSBs of the flight computer address to enable status flags to be dumped onto the 8-bit PC-104 data bus. The table below details the status indicators from the PC-104 data bus:

DATA BUS	STATUS FLAGS
SD0 (LSB)	Main FIFO EF, Active Low
SD1	Main FIFO HF, Active Low
SD2	Main FIFO FF, Active Low
SD3	Backup FIFO serial output inverted
SD4	Backup FIFO EF, Active Low
SD5	Backup FIFO HF, Active Low
SD6	Backup FIFO FF, Active Low
SD7(MSB)	Main FIFO serial output inverted

6.9 Hardware Configuration

The TDI board uses the same vertical PC-104 bus architecture as the flight computer. The table below details the pins used by the TDI board from the AT bus expansion connector.

PIN	SIGNAL NAME	FUNCTION	IN/OUT	CURRENT
A2	SD7	Data Bit 7	I/O	6mA
A3	SD6	Data Bit 6	I/O	6mA
A4	SD5	Data Bit 5	I/O	6mA
A5	SD4	Data Bit 4	I/O	6mA
A6	SD3	Data Bit 3	I/O	6mA
A7	SD2	Data Bit 2	I/O	6mA
A8	SD1	Data Bit 1	I/O	6mA
A9	SD0	Data Bit 0	I/O	6mA
A21	SA10	Address Bit 10	I/O	6mA
A22	SA9	Address Bit 9	I/O	6mA
A23	SA8	Address Bit 8	I/O	6mA
A24	SA7	Address Bit 7	I/O	6mA
A25	SA6	Address Bit 6	I/O	6mA
A26	SA5	Address Bit 5	I/O	6mA
A27	SA4	Address Bit 4	I/O	6mA
A28	SA3	Address Bit 3	I/O	6mA
A29	SA2	Address Bit 2	I/O	6mA
A30	SA1	Address Bit 1	I/O	6mA
A31	SA0	Address Bit 0	I/O	6mA
A32	GND	Ground	N/A	N/A
B2	RESETDRV	System reset signal	OUT	12mA
B3	+5V	+5 Volt Power	N/A	N/A
B13	IOW	I/O Write	I/O	8mA

7.0 Rotator

7.1 General Description

The Rotator flows serial housekeeping data to the flight computer. The Rotator interface uses two interfaces one of which is to the flight computer while the other is to the WFF-93 serial deck of the PCM (Pulse Code Modulation) encoder for LOS communications.

7.2 Rotator and Flight Computer Interface

The Rotator and flight computer interface transfers and collects data and commands to the Rotator. The flight computer collects will route all Rotator commands and read data from the Rotator through this interface.

7.2.1 Rotator Command Format

Commands sent to the Rotator are formatted using a standard 8-byte command format listed in Appendix A. The Rotator Command format provides 2 command bytes per packet. Command byte 1 is the command ID, allowing 256 discrete commands to be identified by the Rotator. Command byte 2 is the data argument for command byte 1. Once the flight computer receives a command packet whose routing ID matches the rotator ID, the entire 8-byte packet is forwarded to the Rotator. The Rotator is responsible for decoding the command packet.

7.2.2 Rotator Telemetry Packet Format

The Rotator uses a telemetry packet format of 47 bytes listed below:
Byte 1: Sync Byte 1 = FAh
Byte 2: Sync Byte 2 = F3h
Byte 3: Sync Byte 3 = 20h
Byte 4: ID Data Byte: Upper Nibble = Balloon ID = TBD 0h-Fh
Lower Nibble = Rotator Packet ID = 6h
Byte 5: MSB of Data Count = 00h (always)
Byte 6: LSB of Data Count = 28h (always)
Bytes 7-47: Rotator Data Bytes

The Rotator performs its own checksum, and is responsible for formatting data to this format. The flight computer will update its own buffer every 5 seconds with new data from the Rotator and transmit it via the appropriate communication link(s).

7.2.3 Electrical Interface

The electrical interface for the rotator and flight computer uses RS232C. Both the TXD and RXD pins and a common ground are used. The Rotator takes both the TXD and RXD lines into a RS232 UART chip. The pinouts for the Rotator are given below:

Pin #	Description
2	TXD: Transmits Telemetry packet data to the flight computer every 5 seconds
3	RXD: Receives commands from the flight computer

5 Gnd

The TXD and RXD line from the flight computer should be connected to the RXD and TXD lines of the Rotator. Grounds should be shared accordingly.

7.2.4 Protocol

The Rotator protocol for the flight computer interface is listed below:

a) Asynchronous serial utilizing standard NRZ format.
b) One start bit, eight data bits, one stop bit, and no parity.
c) Baud Rate = 2400
d) Data is transmitted least significant bit (LSB) first.

7.2.5 Rotator Update Rates

The Rotator data packet update rate is set to a default of new data every 5 seconds. Changes to the Rotator data rate output are accomplished by routing the "Set Output Interval" command, 1Fh, to the Rotator.

7.3 Rotator and PCM Encoder Interface

The Rotator uses a second interface for testing during the ascent and any high rate data flows requiring the LOS communication link. The Rotator controls the content and format of data sent to the WFF-93 serial deck of the encoder. This interface operates independent of the flight computer interface and is unidirectional to the PCM encoder.

8.0 GPS

8.1 General Description

The GPS interface to the flight computer collects information on the gondola's 3-D absolute position, velocity, altitude, and heading. The flight computer will operate in the request mode. Time, position, velocity and altitude shall be requested from a GPS Ashtech ADU2 unit via an RS232 asynchronous interface from the flight computer.

8.2 Electrical Interface

The flight computer shall use port A or port B from the Ashtech ADU2 for electrical interface connections. Both ports are DB9 connectors. The TXD, RXD and GND lines are the only pins used when wiring the GPS Ashtech ADU2 port to the flight computer comm port. Pin-outs are listed below:

Pin #	Description
2	RXD
3	TXD
5	GND

Input voltage is 12-32VDC on a separate power connector. No on/off switch exists on the GPS Ashtech ADU2. Communications with the Ashtech ADU2 comm ports can be established after the unit has successfully booted.

8.3 Commands

The Ashetch ADU2 classifies command into three categories: Set, Query, and Response. The set, query and response commands are represented by $PASHS, $PASHQ, and $PASHR respectively. All commands must terminate with a carriage return and linefeed. The GPS functional categories are receiver control, attitude control, and raw data commands.

8.3.1 Receiver Control

Receiver control commands communicate with the GPS receiver within the Ashtech ADU2. The flight computer uses the receiver control command for initialization of the GPS receiver and setup of the GPS port for communicating to the flight computer.

8.3.1.1 Setting Raw Data Output Type

The output type for raw data from the Ashtech ADU2 is in either ASCII or Binary format. The Ashtech ADU2 must be told which output format will be used. In general, setting the raw data output type is accomplished using the $PASHS,OUT,x command.

9.0 Line of Site (LOS) TM

9.1 General Description

The Line of Site (LOS) Telemetry (TM) interface to the flight computer flows housekeeping data during the ascent and float time in which the ground tracking receivers and antennas are in site of one another.

10.0 LOS Command

10.1 General Description

The LOS Command (CMD) interface to the flight computer serves as the messaging line between the LOS ground control and the SIP during ascent and float time in which the LOS receivers and antennas are in site of one another.

11.0 INMARSAT

11.1 General Description

The INMARSAT interface to the flight computer flows housekeeping data and is the one of the three OTH communication links.

12.0 HSK and PDU Stacks

12.1 General Description

The Housekeeping (HSK) and Power Distribution Unit (PDU) stack interfaces to the flight computer collect most of the sensor and housekeeping data. The HSK and PDU stacks share an Asynchronous Addressable Receive and Transmit (AART) line. The HSK stack is known as the system stack and will consist of several different data acquisition and command decks. The PDU stack serves to command and monitor the power distribution and data path switching functions.

12.2 System & PDU Stack

The HSK & PDU stacks have a total possibility of as many as 5 different decks: housekeeping, discrete command, power base, TDRSS command decode, and timed command decks. These decks communicate on a vertical bus with each other utilizing AART addressing. This section details how each of the different deck structures interface to the flight computer via a single serial AART line from the power base deck.

12.2.1 HSK Deck

The housekeeping deck(s) have the ability to collect 32 analog and 16 digital channels of data on a single deck. The flight computer must query the HSK deck to extract analog or digital data by using a 2-byte command that returns 2 bytes of data. This process is described in the next section entitled "HSK Data Acquisition."

12.2.1.1 Query Command(s)

Analog or digital data is extracted from the HSK deck by using a 2-byte query command that consists of the AART address and the analog/digital channel from which data is being collected. The first byte is always the AART address while the second represents the analog/digital channel assignment. An example of querying an analog channel from the system stack in hex format is B245. B2 represents the HSK deck address of the system stack while 45 is the analog channel. A complete list of the AART addresses is listed in appendix B.

12.2.1.2 Channel Assignments

The second byte of the HSK query command represents the analog/digital channel from which data is being requested. Appendix B lists all the HSK deck channel assignments. The second byte of the example B245 requests channel assignment 45 or analog channel 6 from AART deck B2. Digital data always uses the channel assignment 00 for each deck.

12.2.1.3 Reading HSK Deck data

2-bytes of analog/digital data is placed on the flight computer's RX line after the query command has been executed. Only 12 bits of analog data are used. The second analog byte's lower nibble is not used and bit 4 of the second byte represents the 9th data bit. Below is a table representation of the 12 analog and 16 digital data bits returned by the HSK deck.

Analog Message:

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Byte 1	0	1	2	3	4	5	6	7
Byte 2	x	x	x	x	8	9	10	11

Digital Message:

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Byte 1	0	1	2	3	4	5	6	7
Byte 2	8	9	10	11	12	13	14	15

12.2.2 Discrete Command Deck

The discrete command decks provides up to 28 active low outputs for latching relays for approximately 100ms for each command. Outputs are rated to sink 300mA at 50V maximum.

12.2.2.1 Command Execute

The discrete command deck uses AART addressing in the same manner the HSK decks are used. A 2-byte command must be sent to the discrete command deck requesting a command channel to activate. The first byte is always the AART address while the second is the command channel. Appendix B contains the AART addresses and below is a listing of the 28 command channels hex addresses:

Command Channel #	Hex Address	Command Channel #	Hex Address
Channel 1	09	Channel 15	21
Channel 2	0A	Channel 16	22
Channel 3	0B	Channel 17	23
Channel 4	0C	Channel 18	24
Channel 5	0D	Channel 19	25
Channel 6	0E	Channel 20	26
Channel 7	0F	Channel 21	27
Channel 8	11	Channel 22	41
Channel 9	12	Channel 23	42
Channel 10	13	Channel 24	43
Channel 11	14	Channel 25	44
Channel 12	15	Channel 26	45
Channel 13	16	Channel 27	46
Channel 14	17	Channel 28	47

As an example, the flight computer command A641 is requesting the system stack's discrete deck #1 to activate channel 22. A6 represents the AART address of the system stack's discrete deck #1 and 41 represents discrete command channel 22.

12.2.2.2 Command Echo

The discrete command deck responds to the flight computer via an echo confirming receipt of the command. The AART address and discrete hex channel # address are folded back to the flight computer. The MSB is set to zero and the first byte sent back represents the data (hex channel address) while the second byte is the AART address.

12.2.3 Power Base

The power base is where the serial I/O drivers/receivers are located for communicating with the system stack. The systems stack's ±12V rails and +5V TTL power lines are also generated here. The flight computer's comm port will electrically connect to the power base deck of the system stack. The electrical characteristics of this deck can be found by referencing Physical Science Laboratory's (PSL) manual entitled "Long Duration Balloon Airborne Unit Manual, 1992."

12.2.4 TDRSS Command Decode Deck

The TDRSS command decode deck reformats synchronous commands received from the TDRSS transponder into RS232 equivalent data at 300 baud, no parity, 1 start bit, 1 stop bit, and 8 data bits. The RS232 data is the output of the TDRSS command decode deck and feeds the flight computer's TDRSS CMD comm port. No flight computer interfacing is required for the system stack/HSK comm port to the TDRSS command decode deck. Refer to section 4.0 entitled "TDRSS CMD" for a detailed description of how the flight computer's TDRSS CMD comm port interfaces to TDRSS command decode deck.

12.2.5 Timed Command Deck

The timed command deck allows for time critical commands to be remotely executed from a system that is not real-time oriented. 2-bytes must be sent to the timed command deck to initiate a countdown in 1 Hz increments. The first byte must be the AART address of the timed command deck while the second byte is the timed count is seconds. The second byte is limited to 7 bits and consequently contains a timed count range from 0-127 seconds. The MSB of the second byte should be set high. As an example, the command ACF9 addresses the system stack timed command deck at address AC and causes the output of the timed command deck to stay active low for a period of 121 or F9 seconds whereby the MSB of the second byte is always high. The output of the timed command deck is designed to sink 300mA at 50V maximum. Clamp diodes should be used externally on inductive loads.

13.0 Balloon Control

13.1 General Description

The Balloon Control interface contains the Universal Terminate Package (UTP) housekeeping, UTP primary and backup command, and backup Commandable Apex Package (CAP) housekeeping data. The backup CAP is located on the apex of the balloon. The backup CAP and UTP are considered housekeeping command stacks. Both consists of several decks stacked one upon the other creating a vertical bus structure. This section describes each of these systems and how they interface to the flight computer via an Asynchronous Addressable Receive and Transmit (AART) RS232 line.

13.2 UTP & Backup CAP Electrical Interface

The UTP & backup CAP use an AART RS232 line from the flight computer. The TXD, RXD and ground lines are the only electrical connections necessary. The UTP & backup CAP use a DB9 DTE connector with shielded twisted pair cable. The pin-outs for both systems are the same and given below:

Pin #	Description
2	TXD: Transmits telemetry packet data to the flight computer
3	RXD: Receives telemetry packet data and commands from the flight computer
5	Gnd

13.3 Balloon Control Commanding

Commands sent via the Balloon Control comm port shall flow to the primary or backup command deck of the UTP or the backup CAP command deck. Each system is identified by the routing ID or the lower nibble of byte #2 of the standard 8-byte command packet format listed in appendix A.

The UTP and backup CAP accept 2-byte commands from the flight computer. The flight computer must extract bytes #4 and #6 from the standard 8-byte command packet first before routing them to the command decode deck of the UTP. The first command byte designates the AART address whereby selection of the command decode deck is made. A master list of all the AART address selections is listed in appendix B. Bytes #4 and #6 of the standard 8-byte command format make up the 16-bit command word for the UTP.

13.4 UTP & Backup CAP Protocol

The UTP and backup CAP protocol for the flight computer interface is detailed below:

a. Asynchronous serial utilizing standard NRZ format.
b. One start bit, eight data bits, one stop bit, and even parity.
c. Baud Rate = 4800
d. Data is transmitted least significant bit (LSB) first.

13.5 Balloon Control Data Acquisition Rates

The backup CAP and the UTP require housekeeping data to be acquired by the flight computer at regular intervals. The flight computer shall sample data at a minimum interval of the fastest housekeeping data packet rate. In other words, if INMARSAT executes housekeeping data every 15 minutes then data should be sampled from the backup CAP and UTP stacks at a minimum of every 15 minutes. Likewise, if LOS executes housekeeping data every 20-30 seconds the minimum data acquisition rate from the backup CAP and UTP should be once every 20-30 seconds. The only limit to the maximum data acquisition rates is the CPU processing speed.

13.6 Balloon Control Data Acquisition

This section describes the structure of the data acquisition query commands and how data is read. Data acquisition from the UTP housekeeping deck and the backup CAP are accomplished using AART addressing. The rates at which data is acquired from the backup CAP and the UTP are described in the "Balloon Control Data Acquisition Rates" section 13.5.

13.6.1 Query Commands

Data acquisition commands consist of 2-bytes: an AART address and the analog/digital channel from which data is being requested. The first byte is always the AART address while the second represents the analog/digital channel assignment. An example of querying an analog channel from the UTP housekeeping deck in hex format is B445.

13.6.2 AART Addressing

Reading data from the UTP and/or backup CAP housekeeping deck is accomplished by using AART addressing. The AART address specifies which deck in the UTP or backup CAP stack that data is being queried from. B1 represents the housekeeping deck AART address for the backup CAP stack while B4 represents the UTP housekeeping deck AART address. The first byte will always represent the AART address as in the example given above. A complete list of all AART addresses can be found in appendix B.

13.6.3 Channel Assignments

AART analog and digital channel assignments are listed in appendix B in hex address notation. The channel assignment represents the second byte of the data acquisition command. The example given in 13.6.1 was B445. The second byte (45) represents analog channel 6.

13.6.4 Reading Balloon Control Data

A 2-byte analog data message is sent back to the flight computer once the UTP or backup CAP housekeeping deck has received the analog/digital channel query command. Only 12 bits of analog data are used. The second analog byte's lower nibble is not used and bit 4 of the second byte represents the 9th data bit. Below is a table representation of the 12 analog and 16 digital data bits returned by the housekeeping deck.

Analog Message:

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Byte 1	0	1	2	3	4	5	6	7
Byte 2	x	x	x	x	8	9	10	11

Digital Message:

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Byte 1	0	1	2	3	4	5	6	7
Byte 2	8	9	10	11	12	13	14	15

13.7 UTP HSK Data Packet Format

There are 24 analog channels allocated for UTP and one 16 bit digital word. The flight computer *does not* sample analog channels 1 and 2. All other channels should be sampled accordingly. The UTP complete housekeeping data packet format is listed below:

ANALOG CHANNELS

ANALOG CH #	DESCRIPTION
1	Term Cut Fire Current
2	Aner./BD Fire Current
3	Term. Arm Voltage
4	Ebolt Arm Voltage
5	Aner./BD Arm Voltage
6	Chute Cut Arm Mon
7	Burst Monitor
8	Prim CMD Batt Volts
9	Prim CMD Batt Current
10	B/U CMD Batt Volts
11	B/U CMD Batt Current
12	Telem Batt Volts
13	Telem Batt Current
14	Heater Current
15	Telem TX Temp
16	Circuit Baord Temp
17	Case Temp
18	Battery Temp
19	RFU Temp
20	Spare Temp
21	External Analog1
22	External Analog2
23	External Analog3
24	Spare

DIGITAL CHANNELS

DIGITAL BIT #	DESCRIPTION
0	Cut Wire Mon
1	Expl bolt Fire Mon
2	Aneroid fire Mon
3	HE Valve Status
4	Modem A Active
5	Modem B Active
6	+5VA Present
7	+5VB Present
8	+5VC Present
9	External DIG Input 1
10	External DIG Input 2
11	External DIG Input 3
12	External DIG Input 4
13	Chute Motor Monitor
14	Spare
15	Spare

ULDB UTP housekeeping data packet requirements are not anticipated to change significantly. Cognizant UTP housekeeping data personnel should be contacted to verify format requirements. Currently only one HSK deck is needed to query the UTP for these data elements.

14.0 Primary CAP

14.1 General Description

The Primary CAP or Commandable Apex Package processes data from the primary Top stack and the flight computer. The primary CAP uses a processor to collect data from the flight computer and the primary Top Stack. Data collected is forwarded to the flight computer for transmission. This section describes how the primary CAP processor interfaces with the flight computer.

14.2 Primary CAP Data Flow

The primary CAP requires GPS and MKS data from the flight computer during ascent and float. The primary CAP processor adds information to the initial flight computer telemetry packet by collecting data from the primary Top stack. The CAP processor transmits this telemetry packet back to the flight computer for transmission.

14.2.1 CAP processor to Flight Computer Update Rates

The primary CAP transmits data to the flight computer at 1Hz and 0.2Hz during ascent and float respectively. A command will be sent requiring the CAP to slow down its update rate for float to 0.2 Hz. The flight computer should look for the command that changes the CAP data packet update interval to allow CAP data to be read by the flight computer at the same intervals it is updated from the CAP. CAP data packet interval changes are described under 14.2.3. The primary CAP is responsible for changing its update rates once the flight computer routes the command to the CAP processor.

14.2.2 Flight Computer to Primary CAP Update Rates

The flight computer to the primary CAP telemetry data packet update rate is 1Hz and 0.2Hz during ascent and float respectively. The flight computer is responsible for changing the primary CAP telemetry data packet update rates for MKS and GPS data.

14.2.3 Primary CAP Data Packet Interval Changes

Changes in the primary CAP's update rates are accomplished by using the command 1Fh in command byte 1 of the standard 8-byte command format. Command byte 2 shall have the interval update rate in seconds (i.e. 00000001 = 1 Hz and 00001010 = 0.1 Hz). A change in the primary CAPs update rate is a good indication that LOS data is about to terminate soon. The flight computer must look for this command before initiating a flight computer to CAP update rate change. The flight computer should route the primary CAP packet interval command to the CAP processor and then initiate a flight computer to primary CAP data rate interval change on the flight computer.

14.3 Primary CAP HSK Data Packet Format

The primary CAP adheres to a 47-byte housekeeping (HSK) data packet format. The flight computer is should look for the correct sync bytes and total number of data bytes in the primary CAP HSK data packet. Below is the complete CAP HSK data packet format:

Packet Description		Start Position	Length	From Flight Computer
SYNC 1	Fah	0	8	X
SYNC 2	F3h	8	8	X
SYNC 3	20h	16	8	X
Balloon Address	(0-F)h	24	4	X
Routing Address	6	28	4	X
Data Byte Count	0	32	8	X
Data Byte Count	40 (decimal)	40	8	X
GPS Velocity Up		48	32	X
MKS Lo (Primary)		80	12	X
MKS Mid (Primary)		92	12	X
MKS Hi (Primary)		104	12	X
MKS Mid (Back-up)		116	12	X
MKS Hi (Back-up)		128	12	X
Mid (Primary) Select		140	1	X
Mid (Back-up) Select		141	1	X
Hi (Primary) Select		142	1	X
Hi (Back-up) Select		143	1	X
Lo (Primary) Select		144	1	X
Unused bits		145	7	
DPT 1		152	12	
DPT 2		164	12	
DPT 3		176	12	
DPT Avg		188	12	
PT Selected		200	12	
Misc Flags		212	12	
Command Verify		224	12	
MKS Avg		236	12	
elapsvent in ascent		248	12	
timevent in ascent	brain +30V in float	260	12	
DPT Temp		272	12	
LDBV Pack. Temp		284	12	
Top Plate Temp		296	12	
He Valve Status		308	12	
Control Velocity	dp lower limit in float	320	12	
Max. Allowable Vel. in ascent	dp upper limit in float	332	12	
Delaytim in ascent	dp #3 temp in float	344	12	
HTR & Misc Flags		356	12	
Checksum		368	8	X

The column "From Flight Computer" denotes the data that must be sent from the ULDB flight computer to the CAP processor. The remaining bits in the packet must be set to 0 when forwarding data to the primary CAP. The primary CAP processor is limited to a total of 40 data packet bytes. The primary CAP has the liberty to change the contents of the 40-byte data packet. The flight computer should not expect the contents of the data it sent to the primary CAP to be the same when receiving the 40-byte data packet from the primary CAP. The flight computer should look for the first 3 sync bytes, balloon and routing address, and the data count bytes to remain the same.

Note: The primary HSK data packet format listed above is preliminary and subject to change. Contact primary CAP team to ensure latest format.

14.4 Primary CAP Command Routing

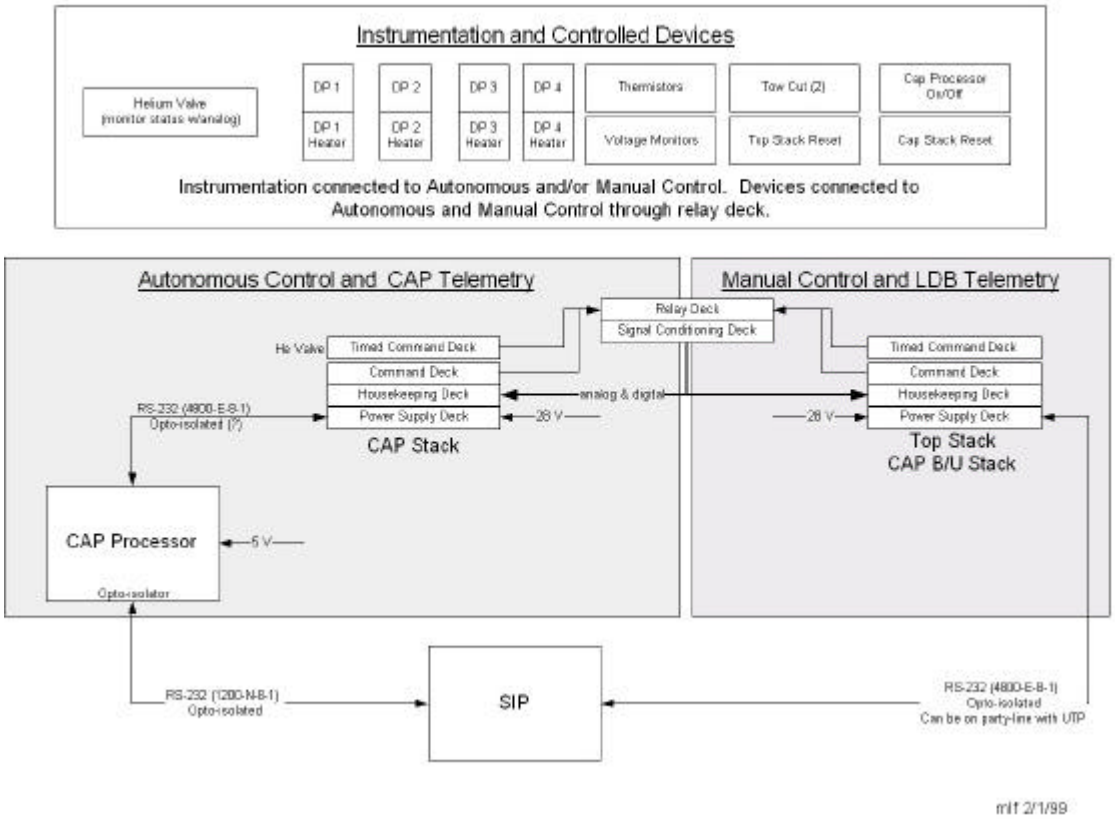
The primary CAP uses the standard 8-byte command packet format listed in Appendix A. The primary CAP is responsible for decoding the 8-byte command packet sent from the flight computer. All commands received from the flight computer will be logged.

14.5 Primary CAP Protocol

The primary CAP protocol for the flight computer interface is detailed below:

e. Asynchronous serial utilizing standard NRZ format.
f. One start bit, eight data bits, one stop bit, and no parity.
g. Baud Rate = 1200
h. Data is transmitted least significant bit (LSB) first.

Preliminary CAP System Diagram



15.0 Ground Diagnostics

15.1 General Description

The Ground Diagnostics interface to the flight computer serves as a tool to debug and test any of the flight computer software embedded capabilities.

16.0 Science

16.1 General Description

Science interfaces to the flight computer's SBS 1553B card. All science data and commands shall conform to the 1553B protocol.

17.0 TDRSS Transponder

17.1 General Description

The TDRSS Transceiver interface to the flight computer uses the 1553B bus protocol for mode control and status information.

Appendix: A

8-byte Command Format:

BYTE #	BINARY	HEX	DESCRIPTION
0	11111010	FA	Sync Word 1
1	11110011	F3	Sync Word 2
2	BBBBRRRR	XX	Balloon/Routing Address
3	????????	??	One's Complement of byte 2
4	XXXXXXXX	XX	Command Byte #1 or AART Address
5	????????	??	One's Complement of byte 4
6	XXXXXXXX	XX	Command Byte #2 or Command Select
7	????????	??	One's Complement of byte 6

Balloon Addresses:

COMMAND BYTE #	BINARY	HEX	DESCRIPTION
2	0000XXXX	0X	LDB Balloon 1
2	0001XXXX	1X	LDB Balloon 2
2	0010XXXX	2X	LDB Balloon 3
2	0011XXXX	3X	LDB Balloon 4
2	0100XXXX	4X	Spare
2	0101XXXX	5X	ULDB Balloon 1
2	0110XXXX	6X	ULDB Balloon 2
2	0111XXXX	7X	ULDB Balloon 3
2	1000XXXX	8X	ULDB Balloon 4
2	1001XXXX	9X	Spare
2	1010XXXX	AX	Spare
2	1011XXXX	BX	Spare
2	1100XXXX	CX	Conventional UTP
2	1101XXXX	DX	Spare
2	1110XXXX	EX	Conventional CIP
2	1111XXXX	FX	Spare

Routing Ids:

COMMAND BYTE #	BINARY	HEX	DESCRIPTION
2	XXXX0010	X2	Science CPU #1
2	XXXX0011	X3	Science CPU #2
2	XXXX0100	X4	Spare
2	XXXX0101	X5	B/U Flight CPU Command Decode
2	XXXX0110	X6	Spare
2	XXXX0111	X7	Spare
2	XXXX1000	X8	UTP: B/U Term. & Primary Term., Parachute
2	XXXX1001	X9	Spare
2	XXXX1010	XA	Flight CPU #1
2	XXXX1011	XB	Flight CPU #2
2	XXXX1100	XC	Spare
2	XXXX1101	XD	Primary CAP
2	XXXX1110	XE	Rotator
2	XXXX1111	XF	Spare

Appendix: B

AART Addresses:

SYSTEM DESCRIPTION	HEX AART ADDRESSES
Primary Terminate Deck	A1
UTP Primary Command Deck	A2
Backup Terminate Housekeeping Deck	A3
UTP Backup Command Deck	A4
Chute Cutaway Housekeeping Deck	A5
System Stack Command Deck #1	A6
System Stack Command Deck #2	A7
Chute Cutaway Command Deck	A8
Primary Terminate Command Deck	A9
Backup Terminate Command Deck	AA
TDRSS Command Decode Deck	AB
System Stack Timed Command Deck	AC
Top Stack Housekeeping Deck	B1
System Stack Housekeeping Deck #1	B2
System Stack Housekeeping Deck #2	B3
UTP Housekeeping Deck	B4
System Stack Housekeeping Deck #3	B5
System Stack Housekeeping Deck #4	B6
System Stack Timed Command Deck	B7
Top Stack Command Deck	B9
Spare	F1
Spare	F2
Spare	F3
Spare	F7
Spare	F8
Spare	F9

HSK Deck Channel Assignments:

ANALOG CH 1:	40	ANALOG CH17:	50
ANALOG CH 2:	41	ANALOG CH18:	51
ANALOG CH3:	42	ANALOG CH19:	52
ANALOG CH4:	43	ANALOG CH20:	53
ANALOG CH5:	44	ANALOG CH21:	54
ANALOG CH6:	45	ANALOG CH22:	55
ANALOG CH7:	46	ANALOG CH23:	56

ANALOG CH8:	47	ANALOG CH24:	57
ANALOG CH9:	48	ANALOG CH25:	58
ANALOG CH10:	49	ANALOG CH26:	59
ANALOG CH11:	4A	ANALOG CH27:	5A
ANALOG CH12:	4B	ANALOG CH28:	5B
ANALOG CH13:	4C	ANALOG CH29:	5C
ANALOG CH14:	4D	ANALOG CH30:	5D
ANALOG CH15:	4E	ANALOG CH31:	5E
ANALOG CH16:	4F	ANALOG CH32	5F

DIGITAL WORD: 00